



08/28/01

Class	Subclass
ISSUE CLASSIFICATION	

BEST AVAILABLE COPY

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED

04

APPLICATION NO. 09/942328	CONT/PRIOR	CLASS 365 711	SUBCLASS 141	ART UNIT 2818 2186	EXAMINER M. Kim H. Kim
------------------------------	------------	--------------------------------	-----------------	-------------------------------------	---------------------------

APPLICANTS

Padmanabha Venkitakrishnan
Shankar Venkataraman
Stuart Siu

3711

Streamlined cache coherency protocol system and method for a multiple processor single chip device

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)			ISSUE FEE	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.					

Form **PTO-436A**
(Rev. 6/99)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)

(FACE)